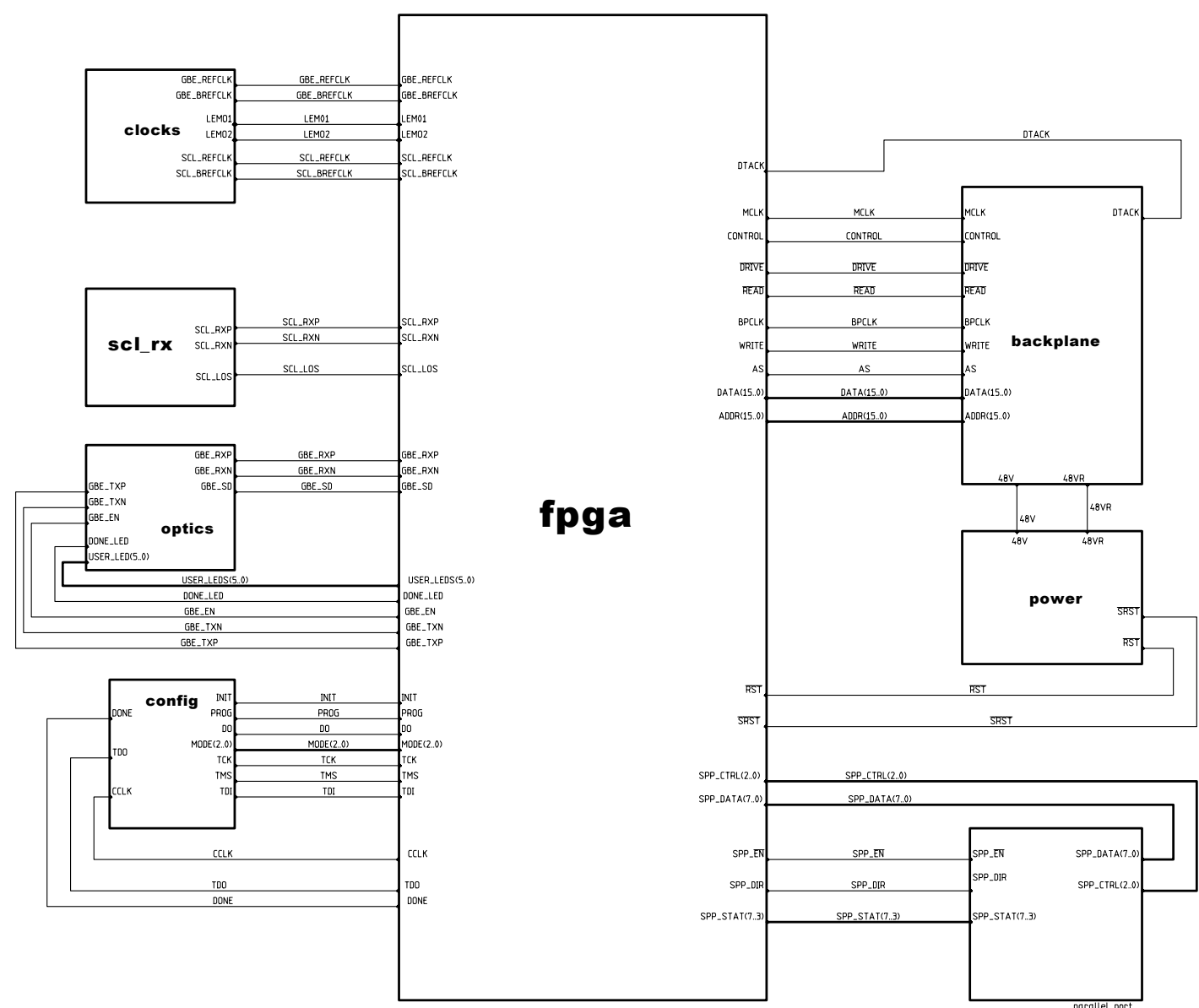

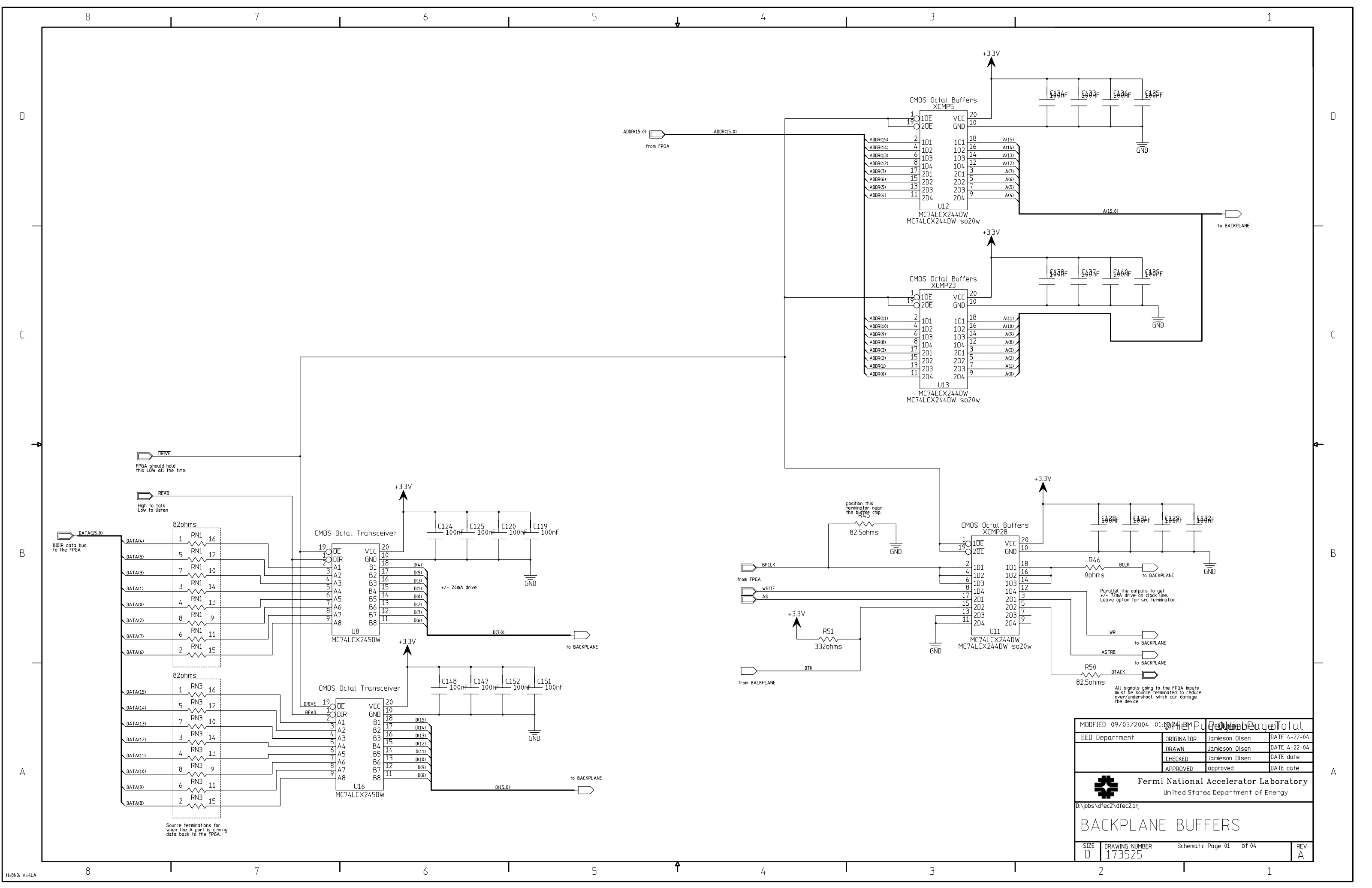



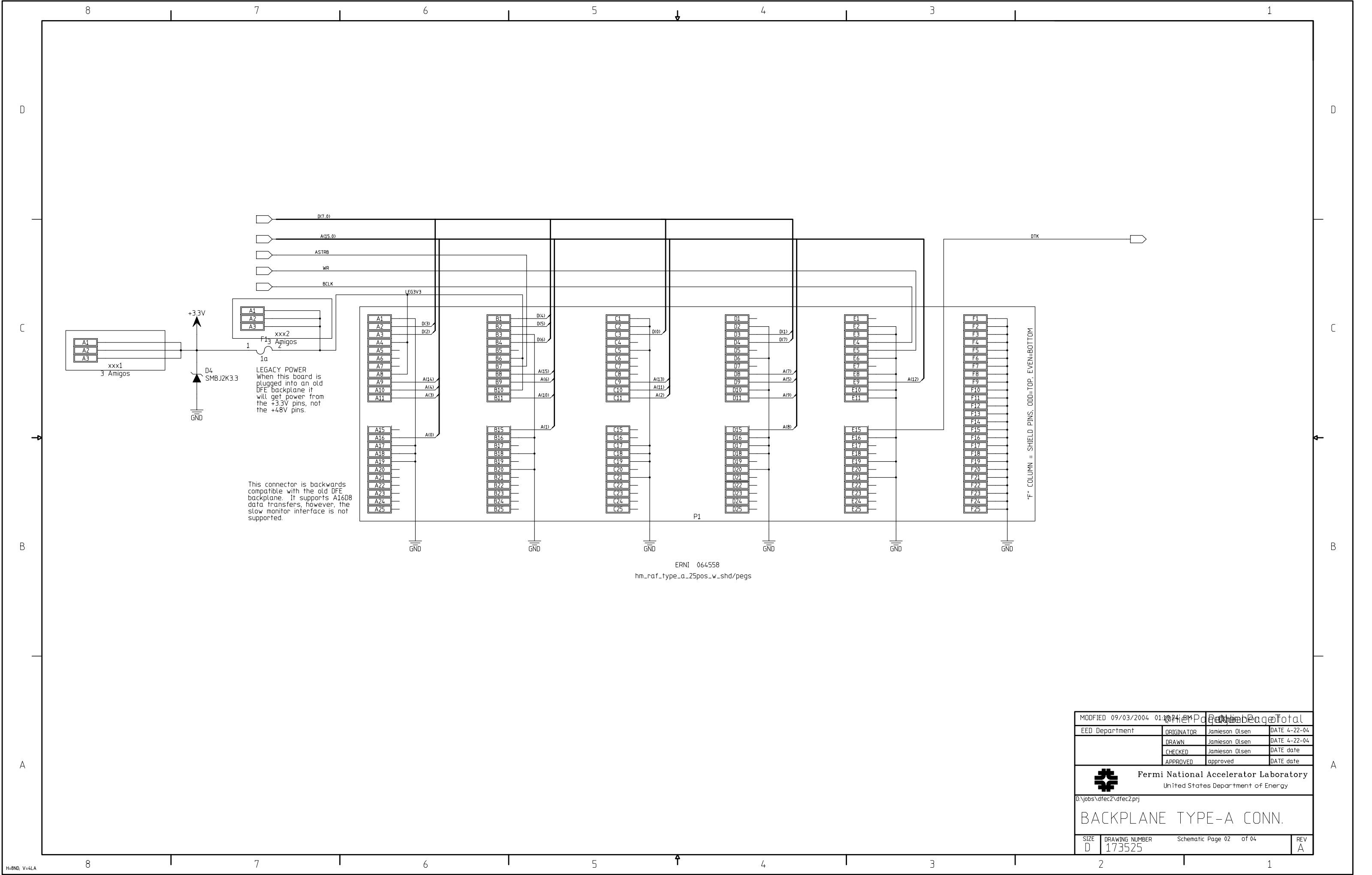
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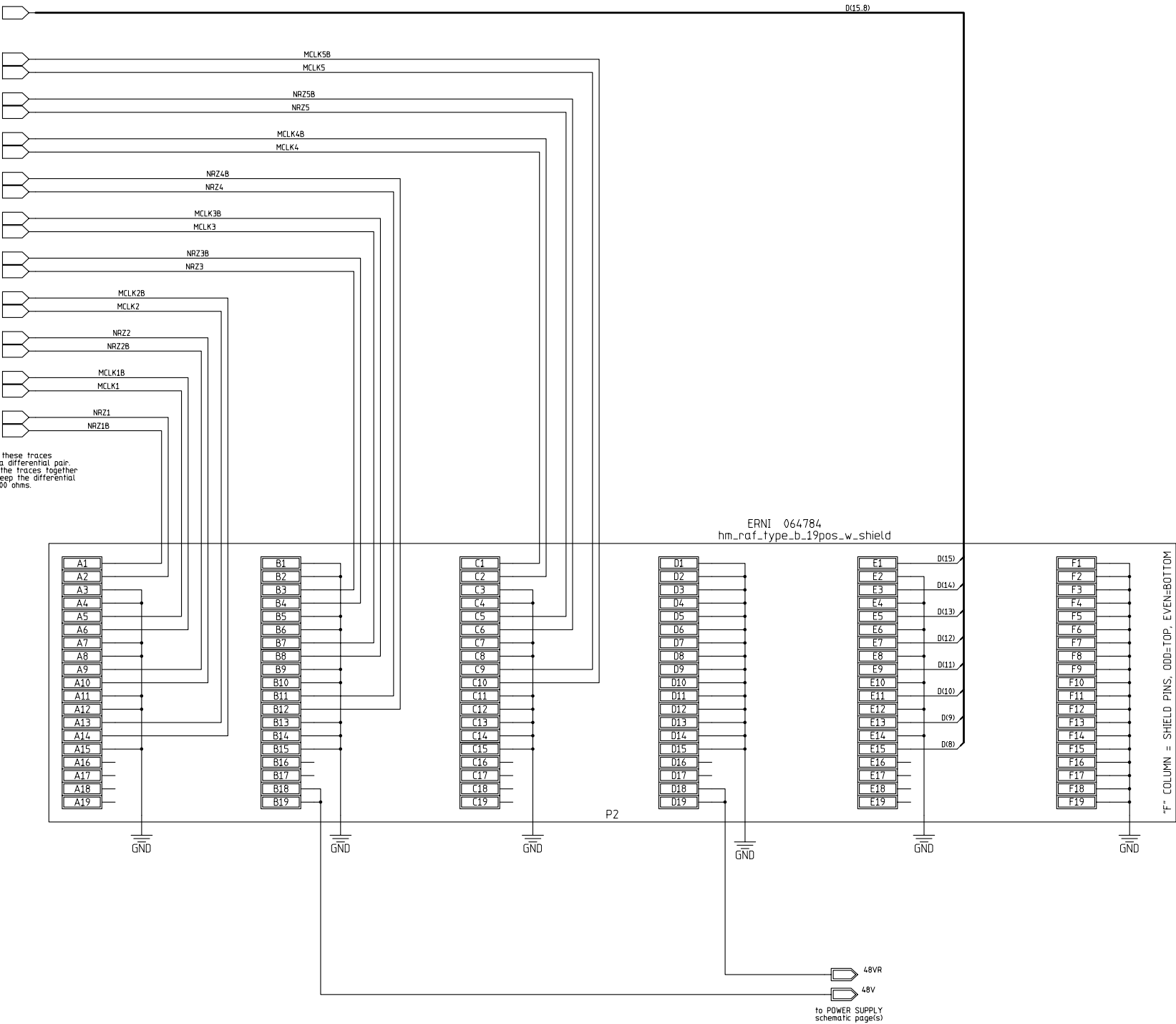
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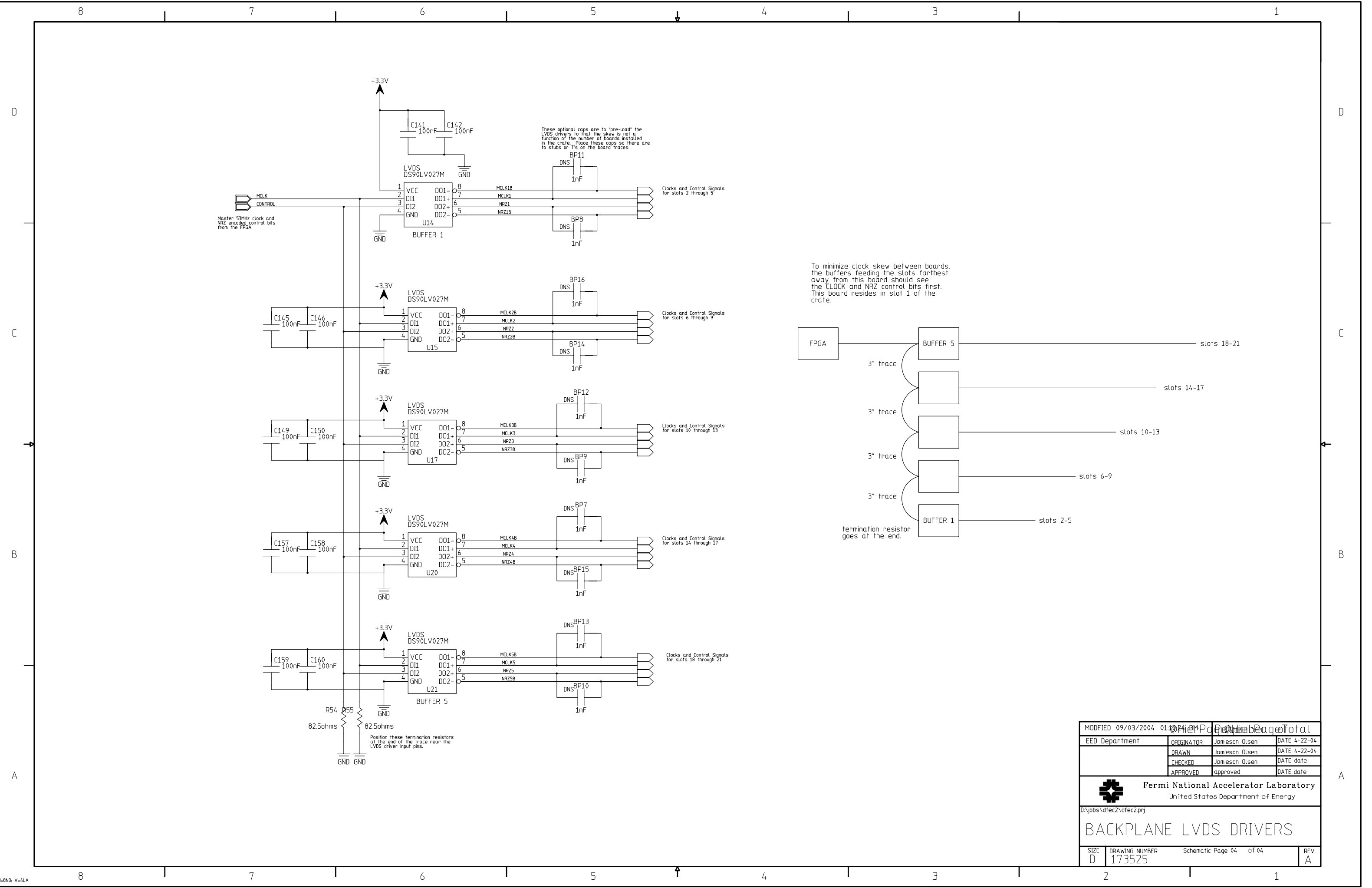
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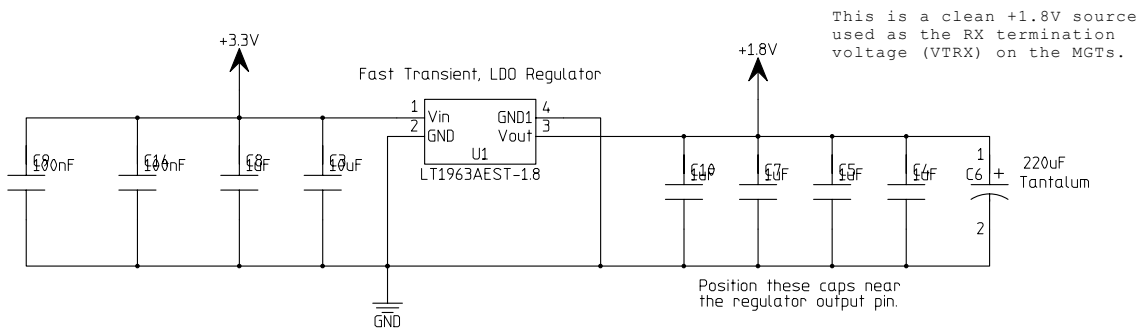
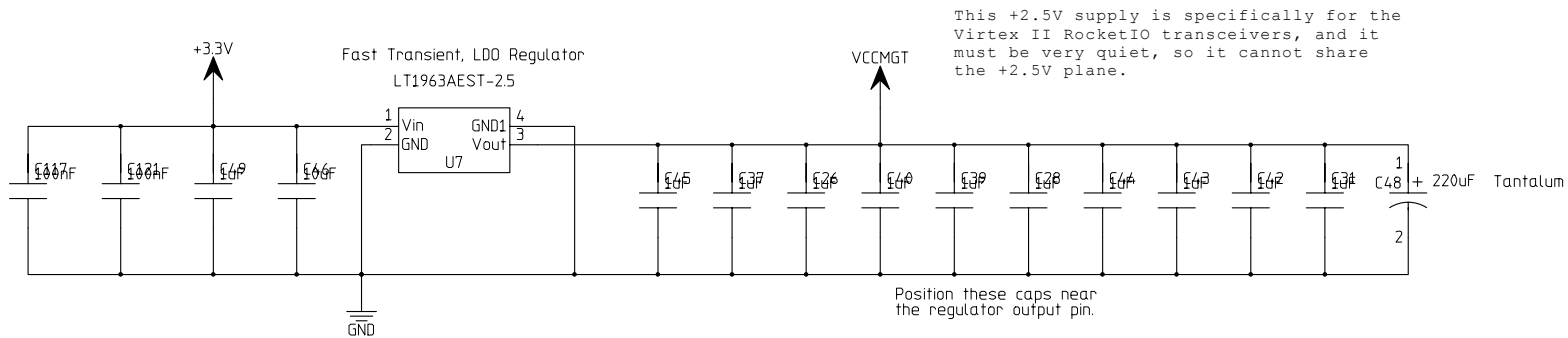
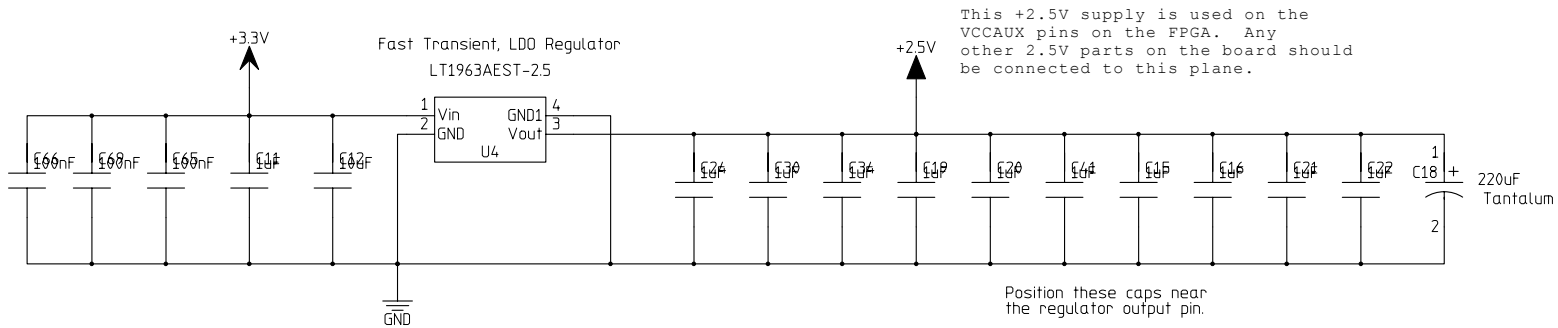
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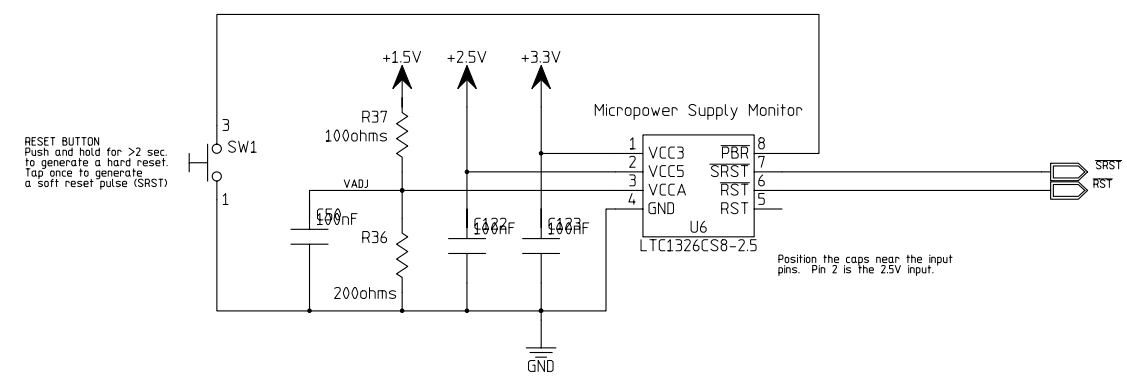
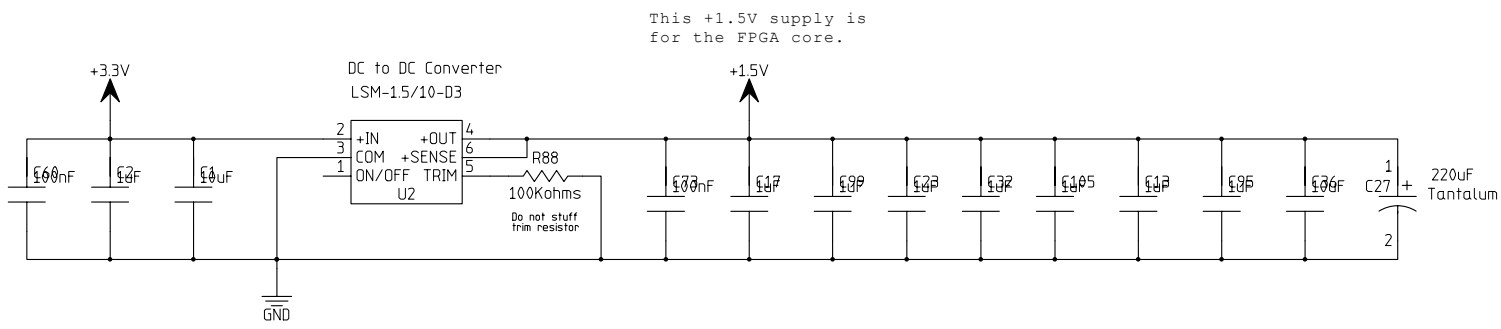
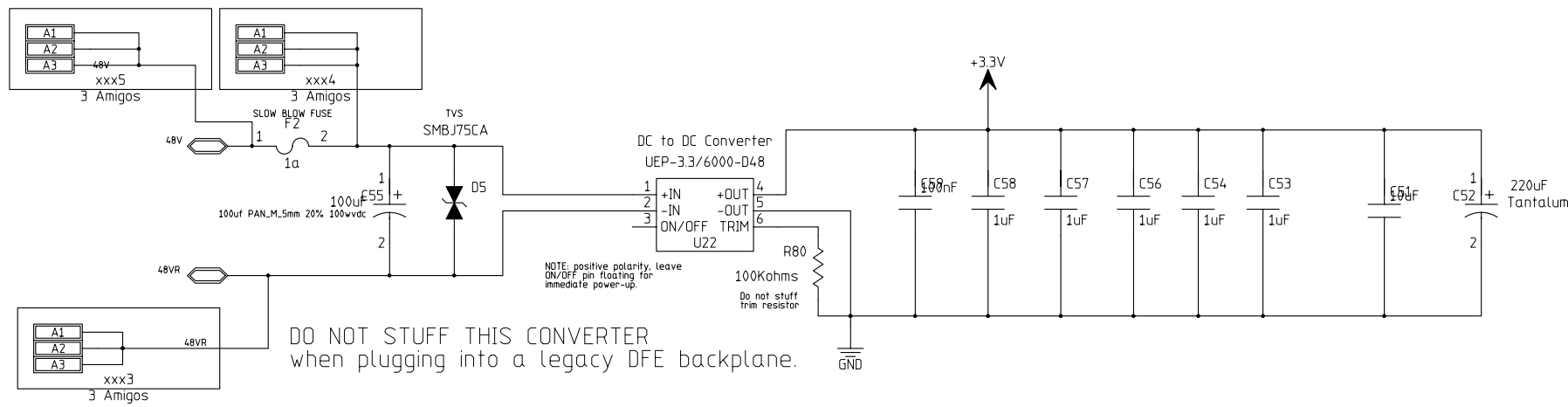
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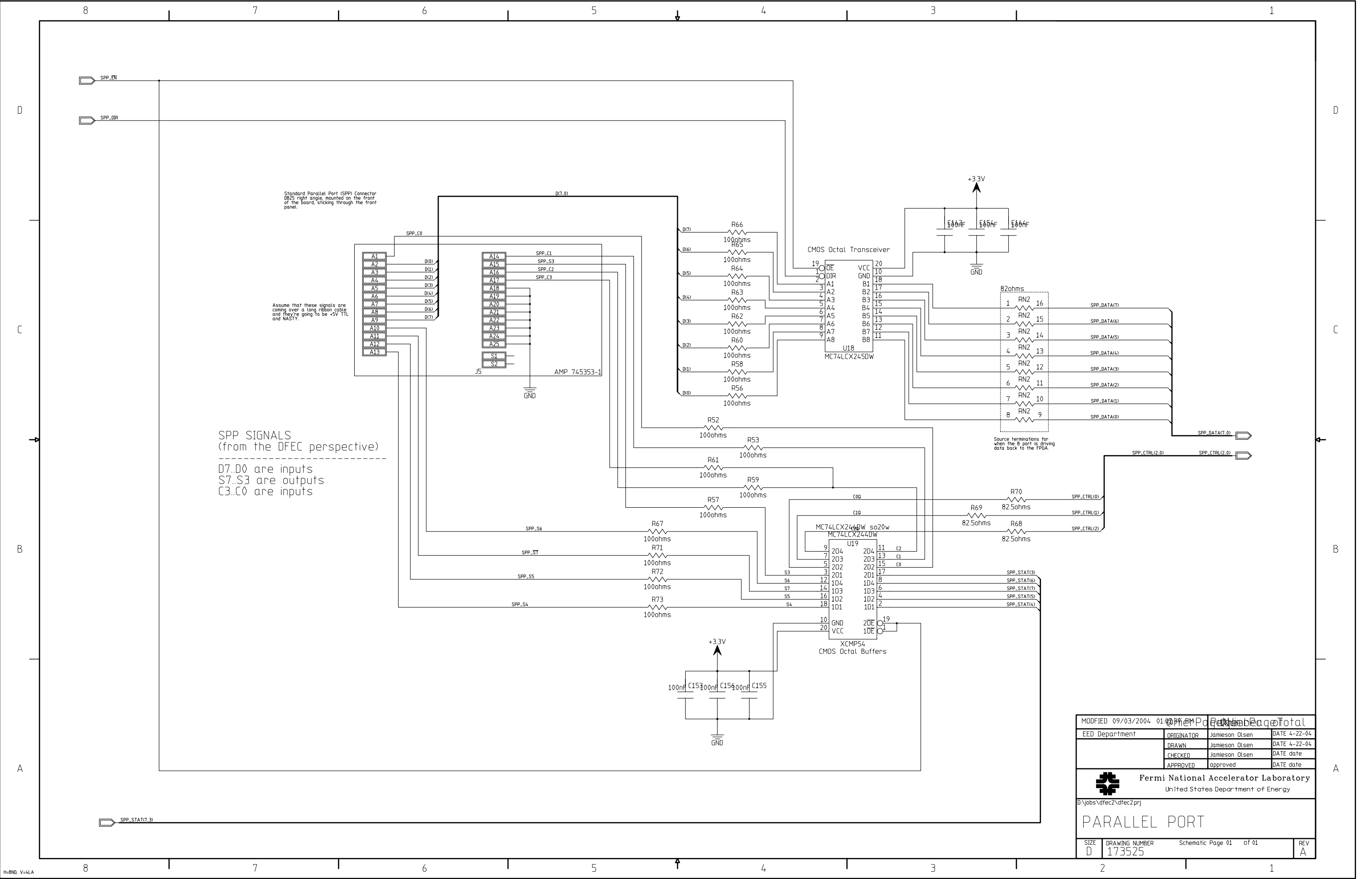
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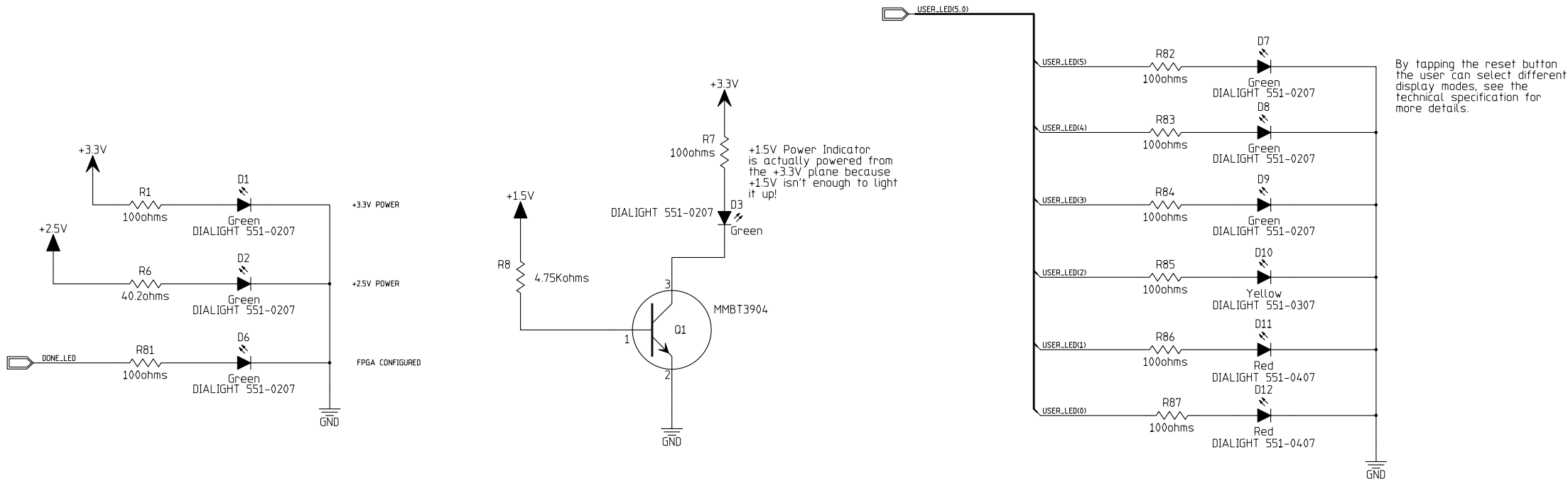
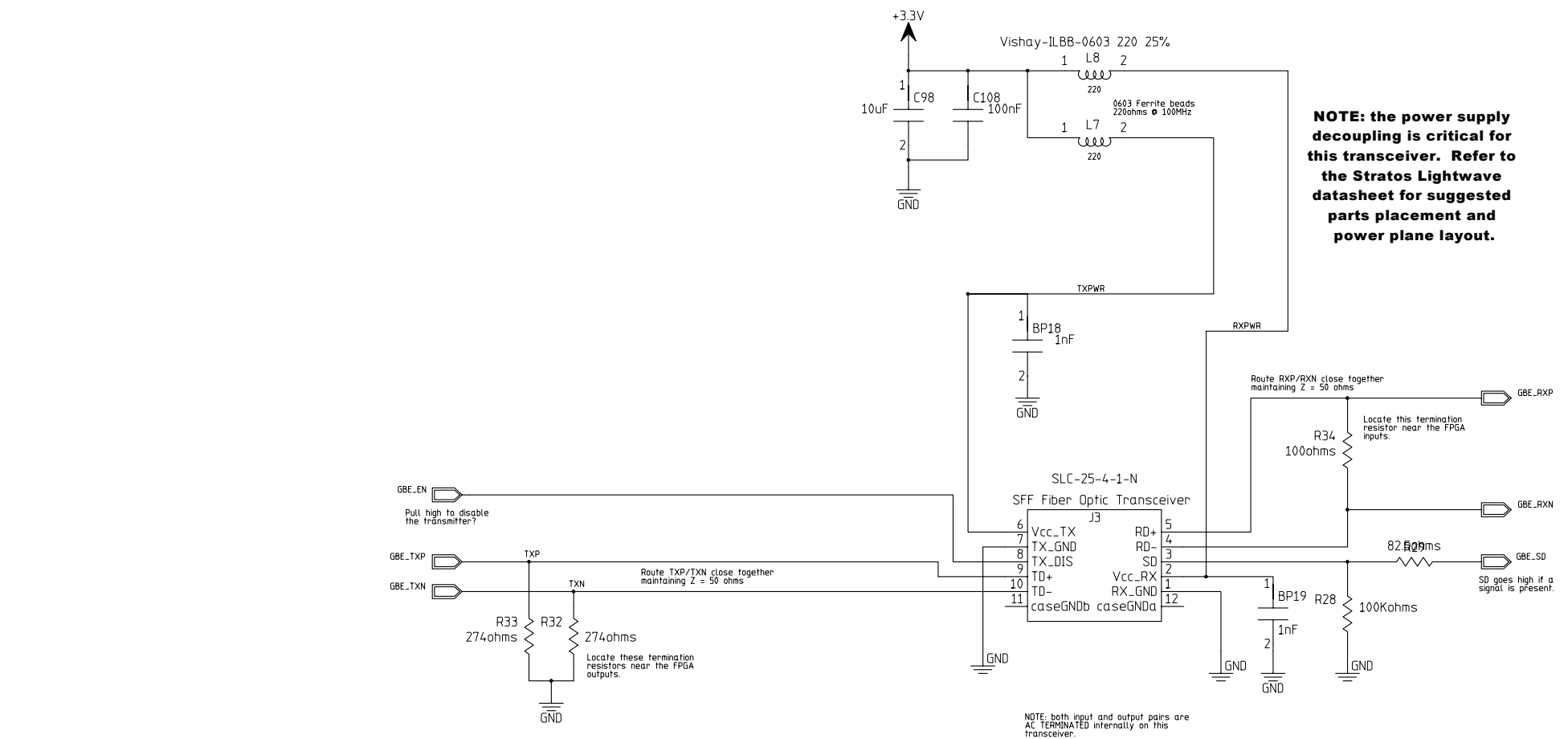
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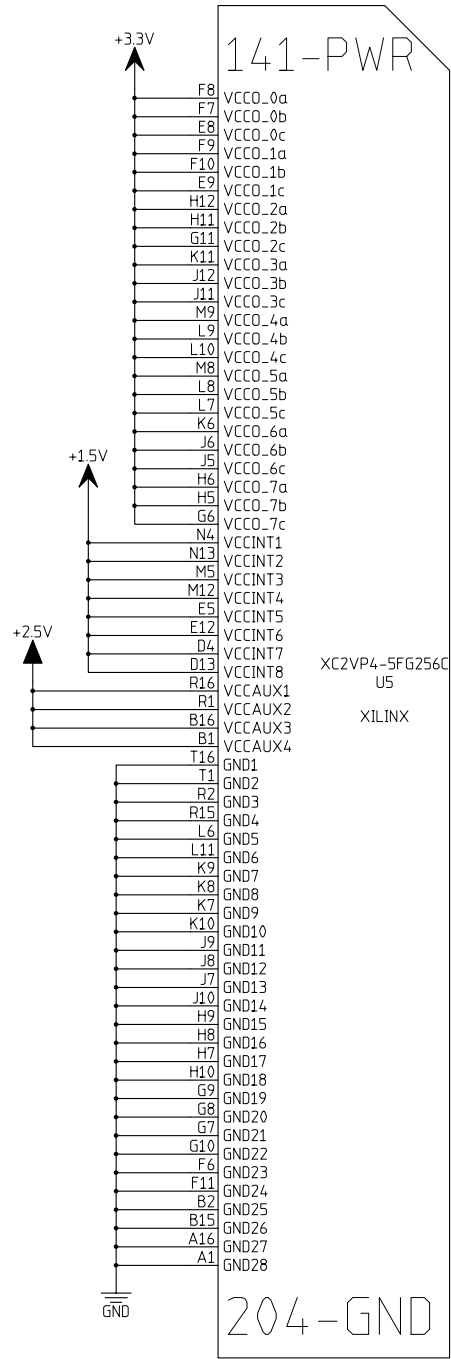
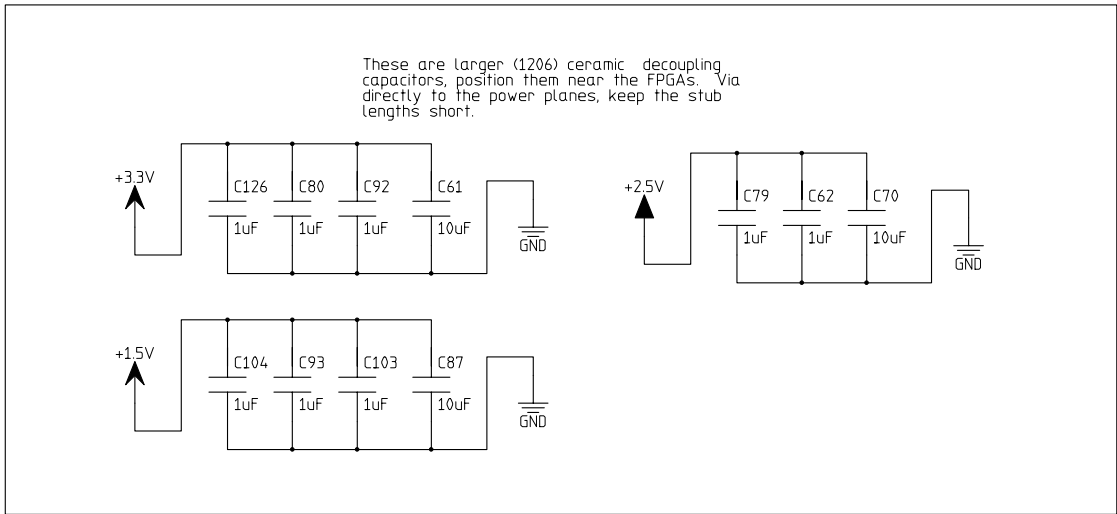
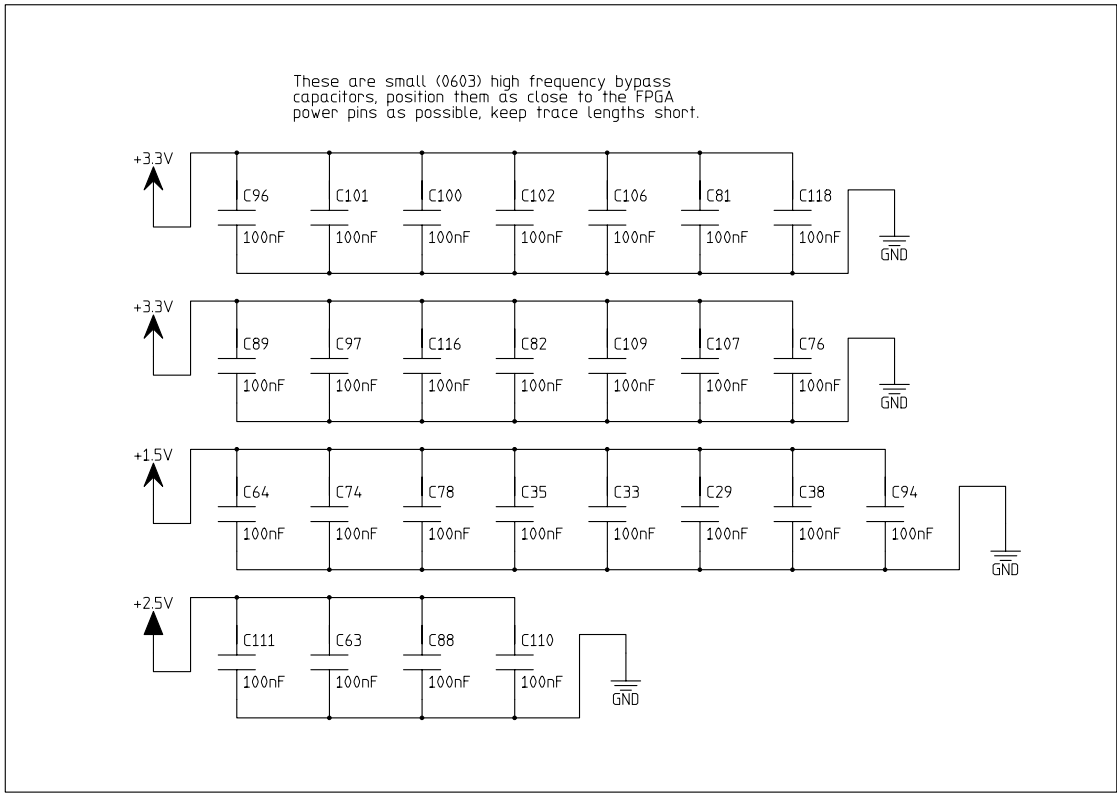
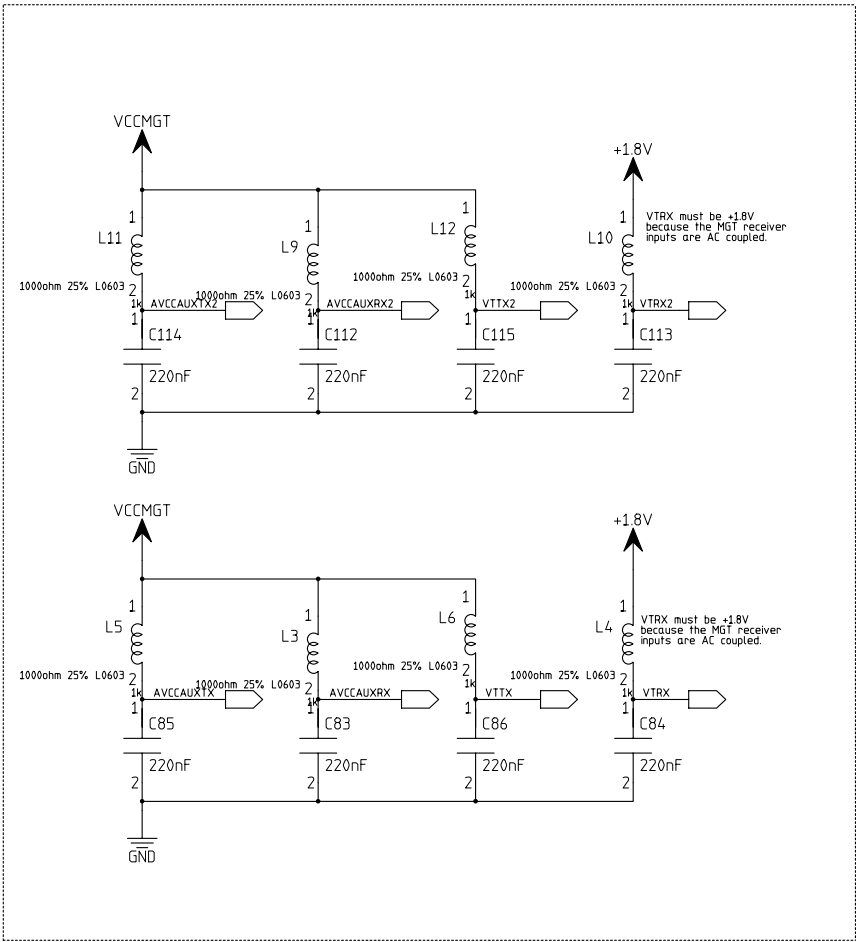
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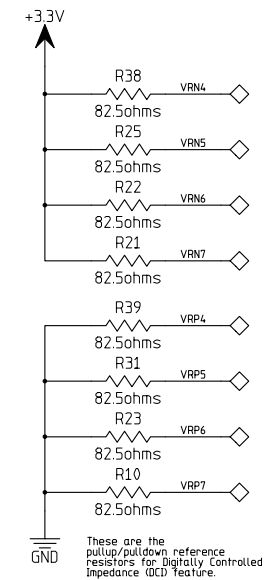
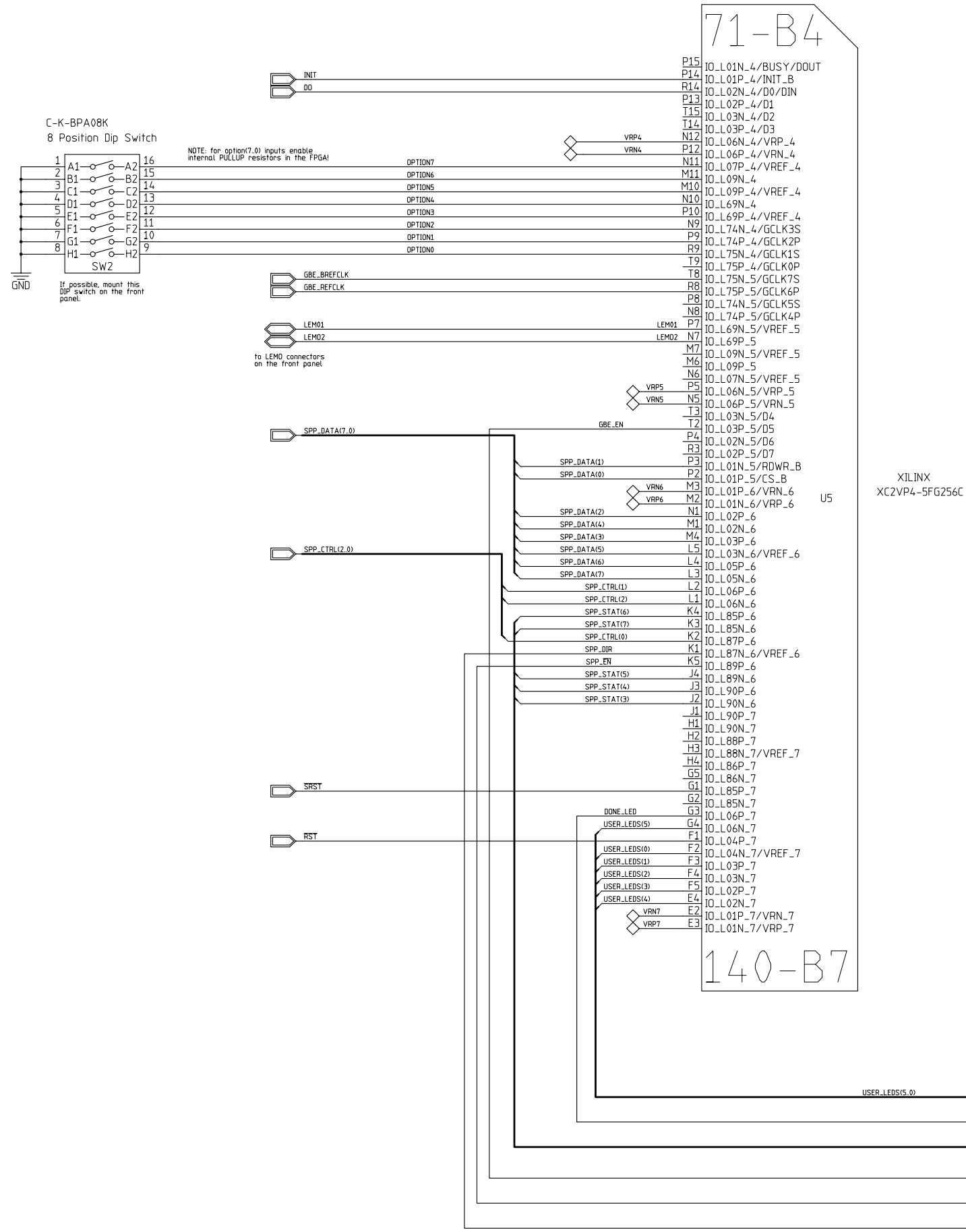



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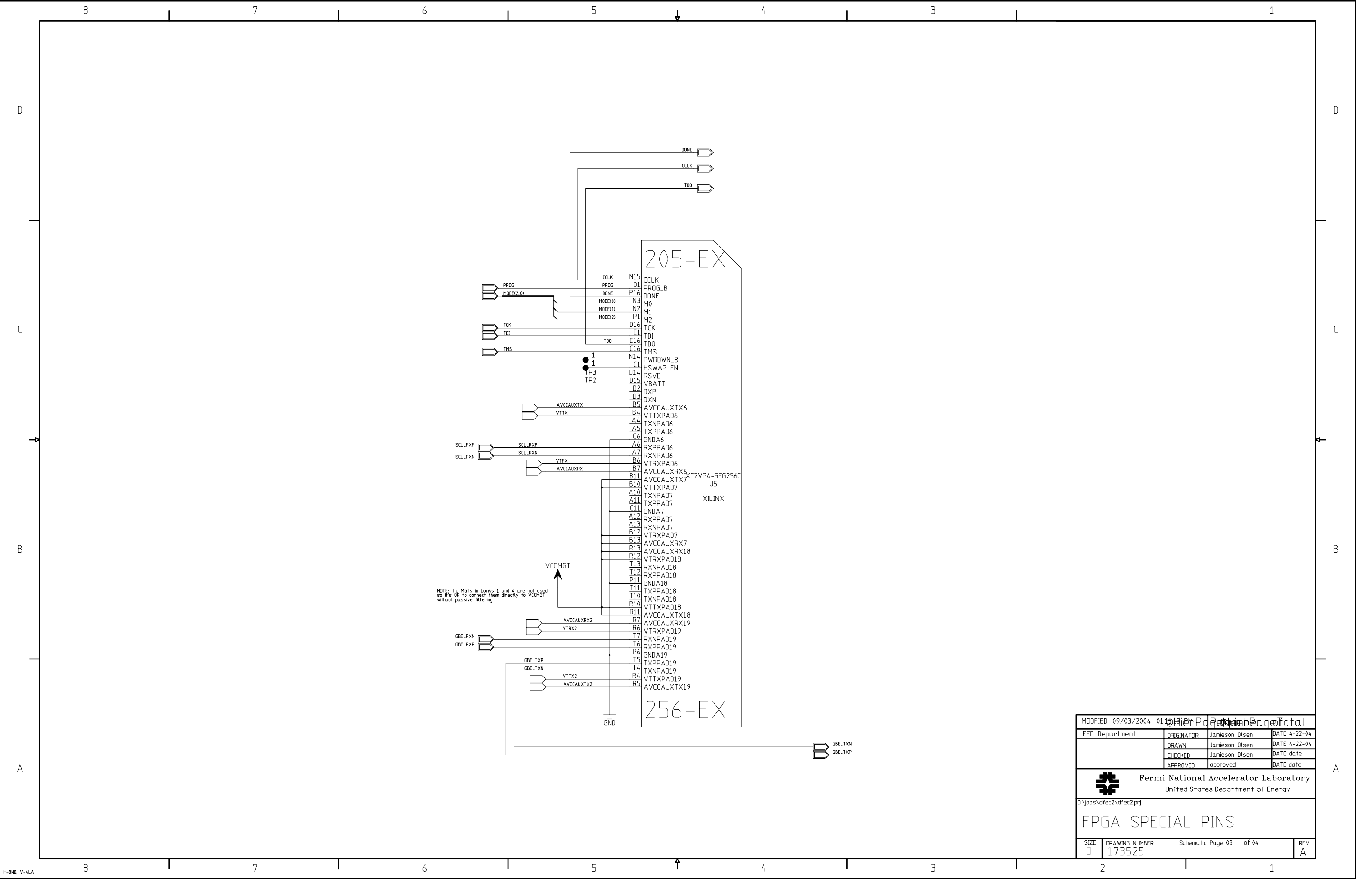


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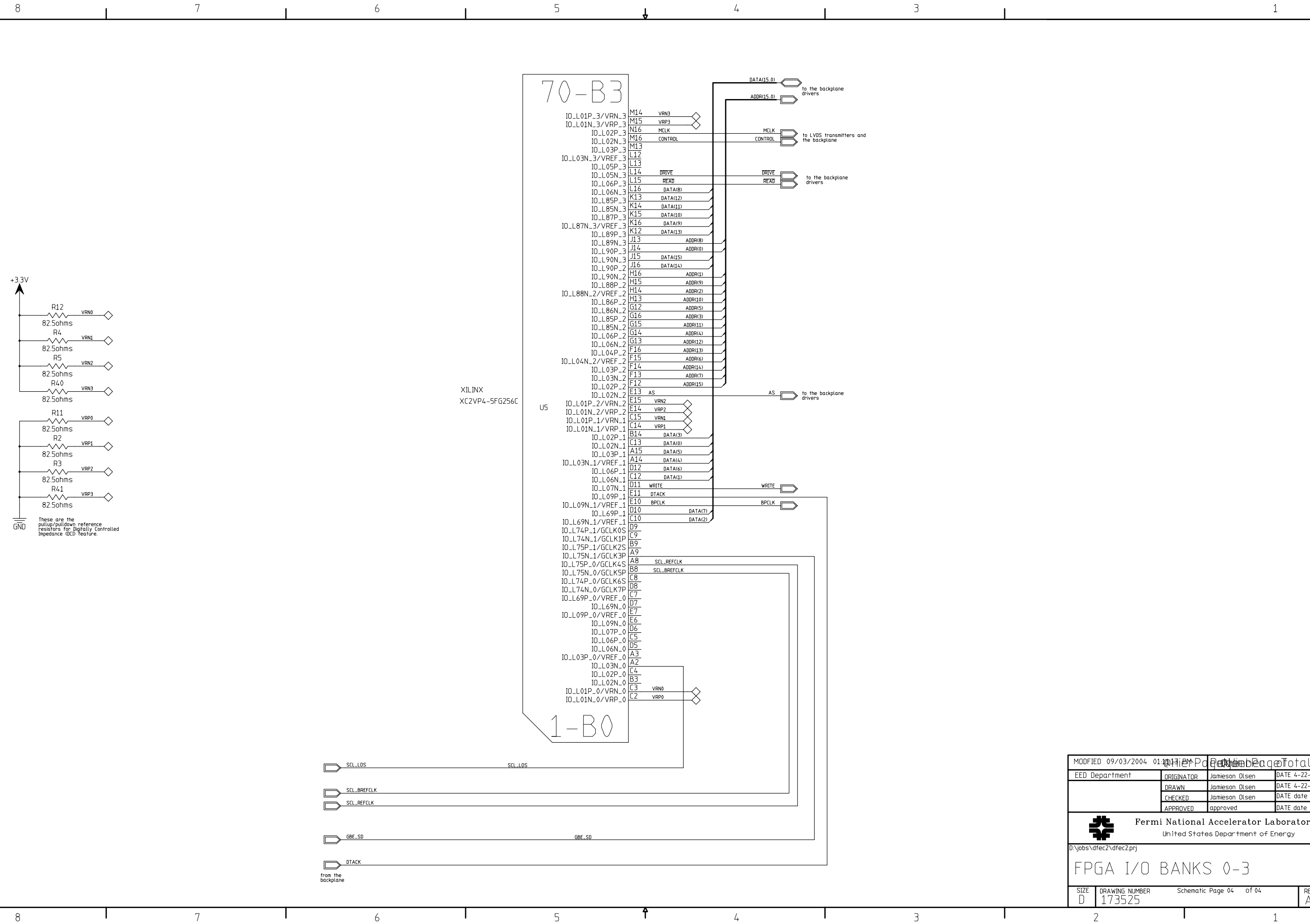
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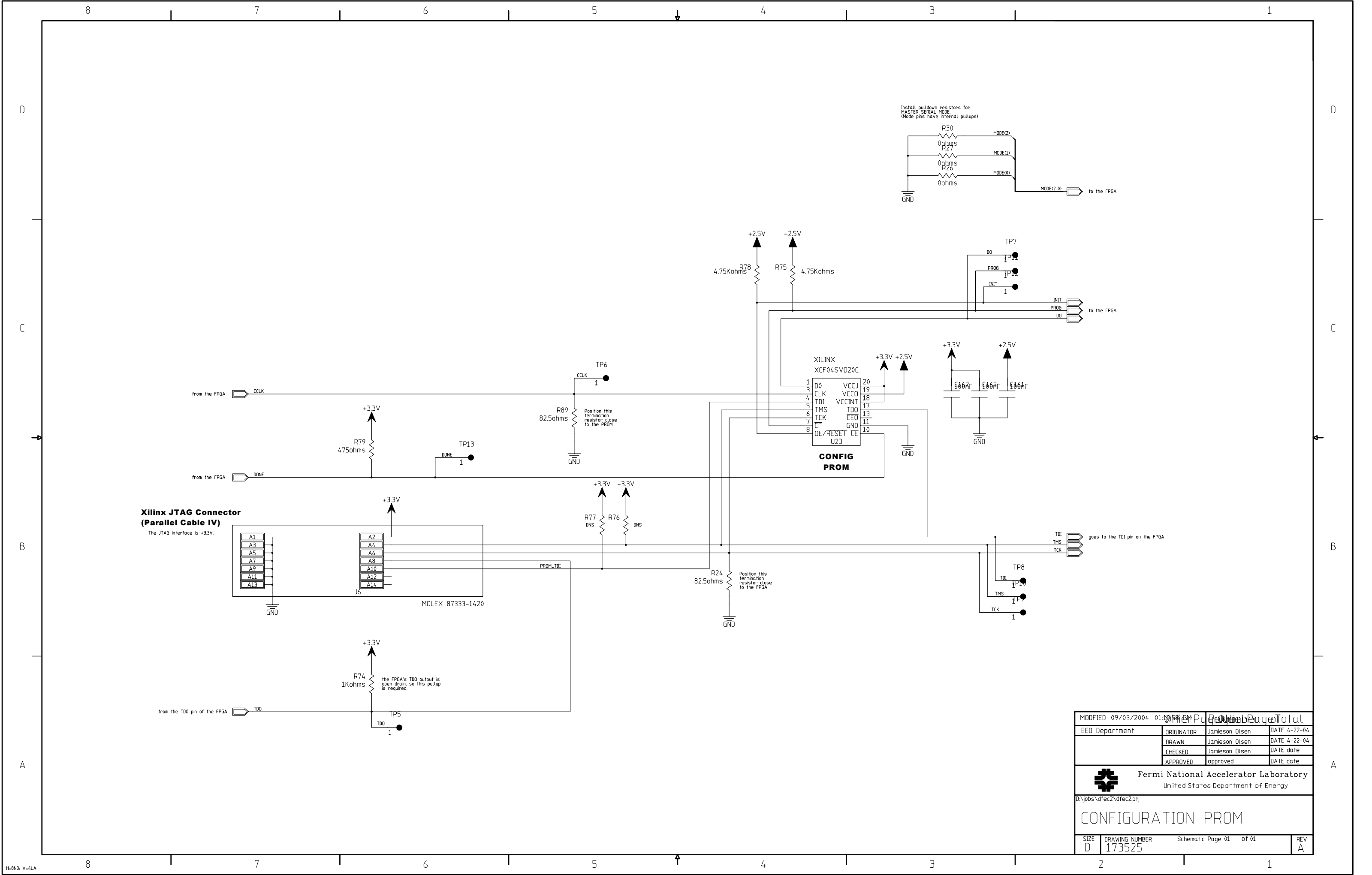
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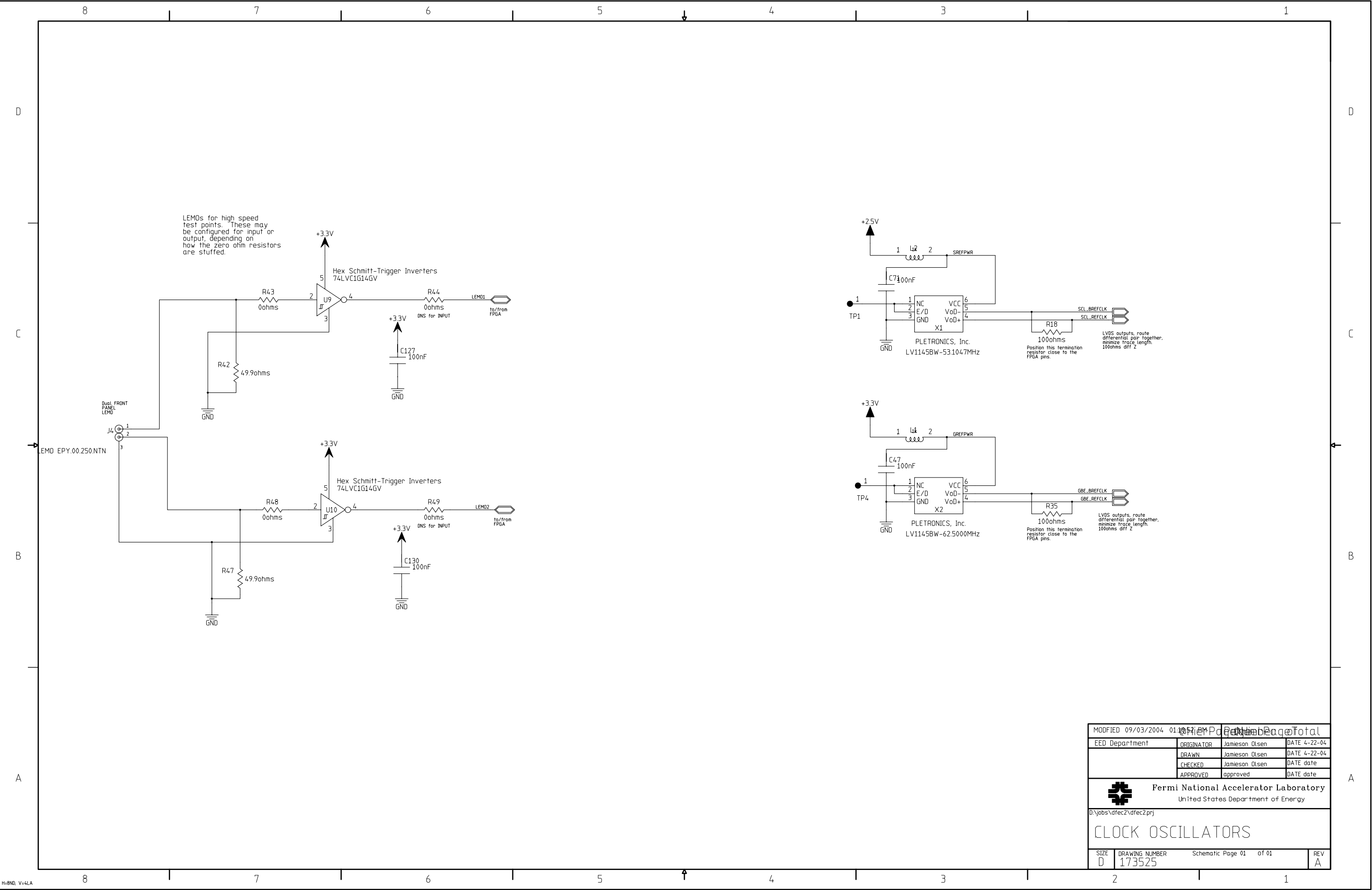
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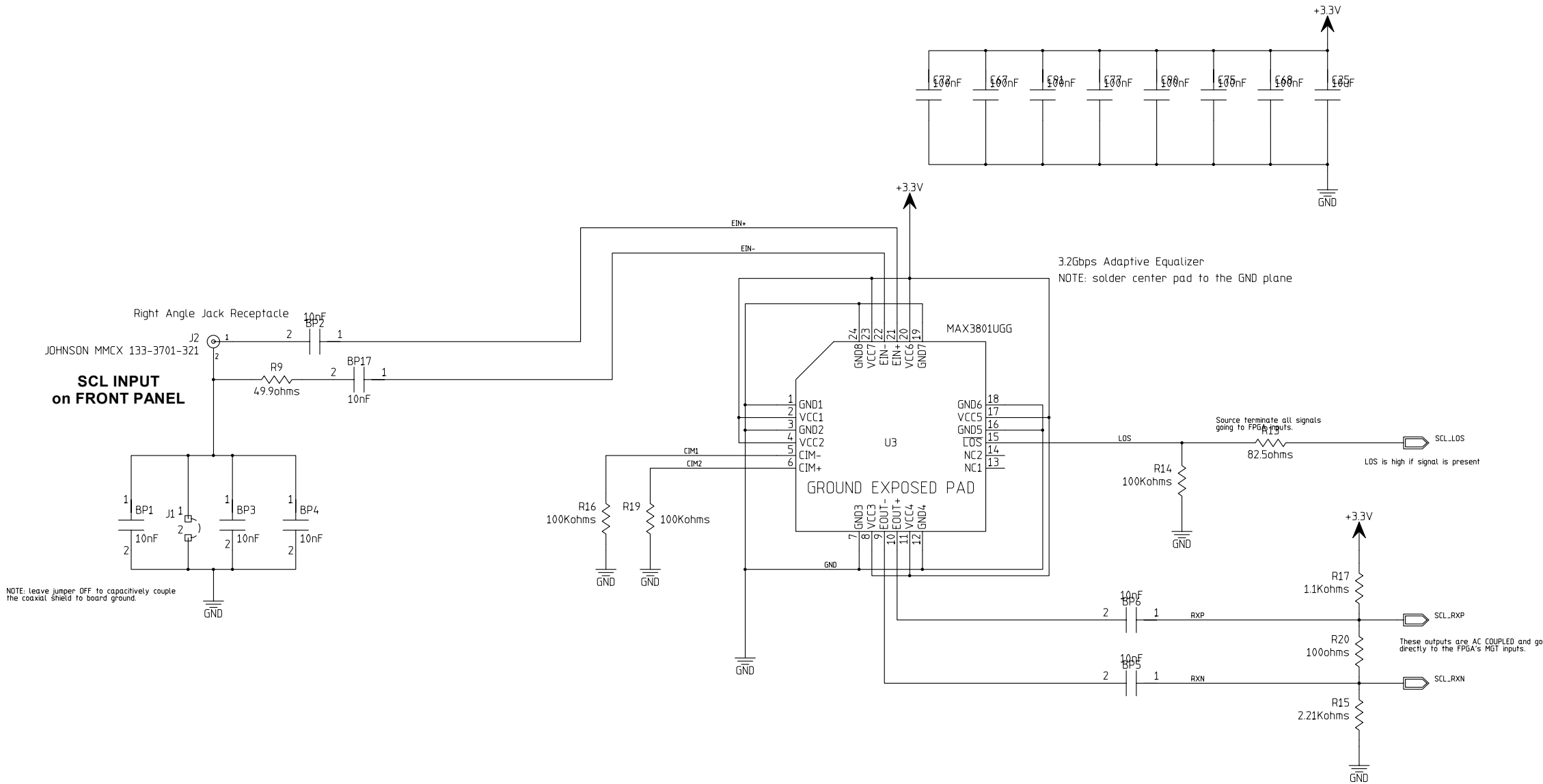


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CONFIGURATION PROM				
SIZE D	DRAWING NUMBER 173525	Schematic Page 01 of 01		REV A






NOTE: Leave jumper OFF to capacitively couple the coaxial shield to board ground.

3.2Gbps Adaptive Equalizer
NOTE: solder center pad to the GND plane

Source terminate all signals going to FPGA outputs.
82.5ohms
LOS is high if signal is present

These outputs are AC COUPLED and go directly to the FPGA's MST inputs.

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SERIAL COMMAND LINK RX			
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